



## PATENT ABSTRACTS OF JAPAN

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**H01L 29/78**(21) Application number: **08298968**(71) Applicant: **NEC CORP**(22) Date of filing: **11 . 11 . 96**(72) Inventor: **YAMAMOTO HIDEO**(54) **SEMICONDUCTOR DEVICE**

(57) Abstract:

**PROBLEM TO BE SOLVED:** To increase the circumference and area, reduce the internal resistance, and enhance the electrostatic strength of, a Zener diode by forming the Zener diode for gate protection along the periphery of a chip, so that its cell region will be encircled.

**SOLUTION:** Polysilicon Zeners 9 are formed along the periphery of a chip 21, so that its cell region 10 will be encircled. The polysilicon Zeners 9 are alternately formed in the direction in which an n<sup>+</sup>-type polysilicon 12, where p-type ion seeds are implanted in polysilicon connects the central portion and peripheral portion of the chip 21 to constitute a kind of Zener diode. The polysilicon Zeners 9 are formed on a silicon substrate 13 with a gate oxide film 14 in-between, and the n<sup>+</sup>-type polysilicon 12 closest to the center of the chip is connected with the source of a transistor through the source Al electrode 16 on the layer-insulating film 15. Thereby the area of the polysilicon Zeners 9 is increased and the internal resistance can be reduced.

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